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Running the Dhrystone 2.1 Benchmark on a Virtex-II Pro PowerPC Processor

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Summary

This application note describes a working Virtex™-II Pro PowerPC™ system that uses the Dhrystone benchmark and the reference design on which the system runs. The Dhrystone benchmark is commonly used to measure CPU performance.

Introduction

The Dhrystone benchmark is a general-performance benchmark used to evaluate processor execution time. This benchmark tests the integer performance of a CPU and the optimization capabilities of the compiler used to generate the code. The output from the benchmark is the number of Dhrystones per second (that is, the number of iterations of the main code loop per second).

This application note describes a PowerPC design created with Embedded Development Kit (EDK) 7.1 that runs the Dhrystone benchmark, producing 600+ DMIPS (Dhrystone Millions of Instructions Per Second) at 400 MHz.

Prerequisites

Required Software

- Xilinx ISE 7.1i SP1
- Xilinx EDK 7.1i SP1
- WindRiver Diab DCC 5.2.1.0 or later

Note: The Diab compiler for the PowerPC processor must be installed and included in the path.

- HyperTerminal

Required Hardware

- Xilinx ML310 Demonstration Platform
- Serial Cable
- Xilinx Parallel-4 Configuration Cable

Dhrystone Description

Developed in 1984 by Reinhold P. Wecker, the Dhrystone benchmark (written in C) was originally developed to benchmark computer systems, a short benchmark that was representative of integer programming.

The program is CPU-bound, performing no I/O functions or operating system calls. The Dhrystone code is dominated by simple integer arithmetic, string operations, logic decisions, and memory accesses intended to reflect the CPU activities in most general purpose computing applications.

The Dhrystone result is determined by measuring the average time a processor takes to perform multiple iterations of a single loop containing a fixed sequence of instructions. When Dhrystone is referenced, it is usually quoted as *DMIPS*, Dhrystone MIPS, or Dhrystones per second. The original Dhrystone benchmark is still widely used to measure CPU performance in the processor industry.

In its evolved application, the Dhrystone benchmark's focus is embedded systems that incorporate floating point calculations. It compares the performance of the processor under

benchmark to the performance of a processor in a reference machine. This provides an advantage over quoting *straight* MIPS numbers because using a reference machine effectively compensates for differences in each processor instruction set.

The VAX 11/780, adopted by the semiconductor industry as the reference 1 MIPS machine, achieves 1757 Dhrystones per second. The Dhrystone figure is calculated by measuring the number of Dhrystones per second for the system and dividing that by 1757. Thus, 80 MIPS means *80 Dhrystone VAX MIPS*, and that means 80 times faster than a VAX 11/780. A DMIPS/MHz rating takes this normalization process one step further, enabling the comparison of processor performance at different clock rates.

Reference Design

The reference design files associated with this application note include four complete EDK design examples for demonstration purposes. Each reference design illustrates the operation of the Dhrystone application code at a different PowerPC core clock frequency. The four clock frequencies are 100 MHz, 200 MHz, 300 MHz, and 400 Mhz. Each of these designs also contains the UCF file and design source for the ML310 Demonstration Platform.

The ML310 Demonstration platform is built around the Virtex-II Pro FPGA and includes the PowerPC 405 Core. The benchmark is run on the PowerPC processor, utilizing the processor caches. The reference design can be targeted to other demonstration boards, but these designs are not provided.

For additional information on the ML310 board refer to the following Xilinx website:

http://www.xilinx.com/ml310.

Complete EDK reference design files for this application note are available on the Xilinx website at:

http://www.xilinx.com/bvdocs/appnotes/xapp507.zip

Hardware

To implement this reference design, use a PowerPC system (created using EDK) that includes the following:

- PowerPC core, including the 16 KB instruction and 16 KB data cache
- Processor Local Bus (PLB), which is connected to a PLB block RAM controller and PLB 16550 UART
- Processor reset block
- JTAG configuration block
- Digital Clock Manager (DCM)

The UART 16550 functions as a STDIN/STDOUT device to query the user and output the Dhrystone benchmark statistics. The PLB block RAM stores the bootloop code. The bootloop code keeps the processor in a known good state until the Dhrystone benchmark is downloaded and run.

Software

The Dhrystone benchmark is provided with a reference design. The reference design includes a software application project named “dhrystone_application”. Associated with this project are three C files, a header file, and a linker script. Table 1 contains a description of the source files.

Table 1: **Dhrystone Source Files**

Source File	Description
config.c	Specifies processor clock speed and sets up the UART
dhry_1.c	Dhrystone source
dhry_2.c	Dhrystone source
dhry.h	Header file for Dhrystone source
dhrystone_linker_script	Maps the Dhrystone benchmark to the PowerPC caches

The Dhrystone benchmark is compiled using a custom Makefile. This Makefile utilizes the Diab compiler to compile and link the benchmark. The Makefile is located in the dhrystone_application directory.

Running the Benchmark

The following procedures describe how to implement the reference design, program the FPGA, download the benchmark, and run the benchmark.

Implementing the Reference Design

1. Unzip the reference design.
2. Launch XPS, and open the system.xmp project.
3. Select **Tools** → **Update Bitstream**.

   The output of the Update Bitstream process is a bit file that is used to configure the Virtex-II Pro FPGA.

Building the Dhrystone Benchmark

In XPS, select **Tools** → **Build All User Applications**.

The output of the build process is the executable and linked format (ELF) file named executable.elf, which is saved in the dhrystone_application directory.

Starting HyperTerminal for Serial Communication

1. Connect the serial cable to ML310 and the host development machine.
2. Start a HyperTerminal program.
3. Specify the following serial port settings:
   - Port: Specify the com port connected to the ML310 UART
   - Baud Rate: 9600
   - Data: 8 bit
   - Parity: none
   - Stop: 1 bit
   - Flow Control: none

Downloading and Running Dhrystone Benchmark

1. In XPS, select **Tools** → **Download.**

2. After the FPGA is configured, select the custom button **!U1**. This starts XMD, downloads the code, and begins executing the benchmark.

Understanding the Dhrystone Benchmark

The Dhrystone code uses the *time ()* system call to measure time with a resolution of whole seconds. At this resolution, the number of iterations run has a direct effect on the accuracy of the Dhrystones per second calculation. The error of the Dhrystone result is 2/(run time in seconds). For example, with the PowerPC processor running at 300 MHz and 30000000 (30 million) iterations, the run time is 36 seconds, resulting in 474 DMIPS. The error rate is ±5% (2/36). To get the error percentage down into the 1% (±0.5%) range, the design must run for 400 seconds, *or* 333333333 (~333 million) iterations.

1. In the HyperTerminal, enter the number of iterations as 333 million.
2. After ~36 seconds, the benchmark finishes and outputs the following:

```
Microseconds for one run through Dhrystone:      1.2
Dhrystones per Second:                         822276.0
```

One common representation of the Dhrystone benchmark is DMIPS, which is obtained when the Dhrystone score is divided by 1757, as follows:

DMIPS = 833333.3/1757 = 474

DMIPS/MHz = 1.56

Table 2 contains the DMIPS values for various PowerPC clock frequencies when running 333 million iterations.

Table 2: **DMIPS Values**

CPU Clock Frequency	Inlining Disabled		Inlining Enabled	
	DMIPS/MHz	Dhrystone MIPS	DMIPS/MHz	Dhrystone MIPS
100 MHz	1.35	135	1.56	156
200 MHz	1.35	271	1.56	312
300 MHz	1.35	407	1.56	468
400 MHz	1.35	542	1.56	628

Conclusion

The Dhrystone benchmark is a general-performance benchmark used to evaluate processor execution time. As illustrated in this application note, the embedded PowerPC core in the Virtex-II Pro delivers 600+ DMIPs with a processor clock rate of 400 MHz.

Revision History

The following table shows the revision

Date	Version	Revision
07/11/05	1.0	Initial Xilinx release.