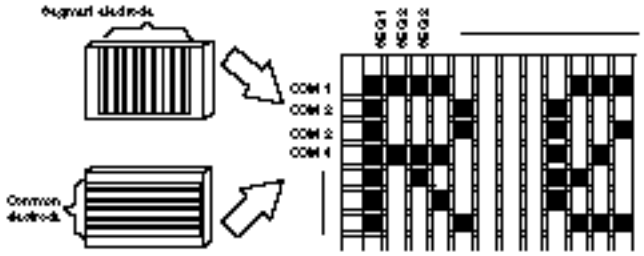
PRINCIPLES OF OPERATION

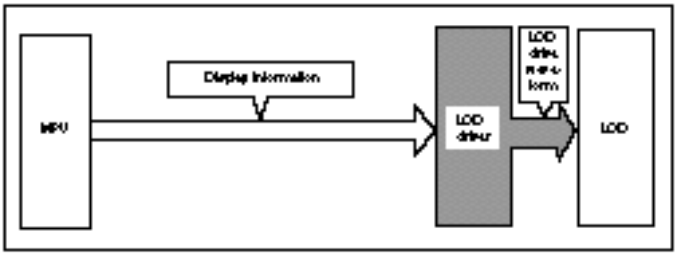
Graphic modules offer the greatest flexibility in formatting data on the display. They allow for text, graphics or any combination of the two. Since character size is defined by software, they allow any language or character font to be shown. The only limit is the resolution of the display.

Graphic modules are organized in rows (horizontal) and columns (vertical) of pixels. Each pixel is addressed individually, allowing any combination to be ON. This bitmapping provides the user with the ability to construct text of any size or shape, or true graphics, if that is desired.

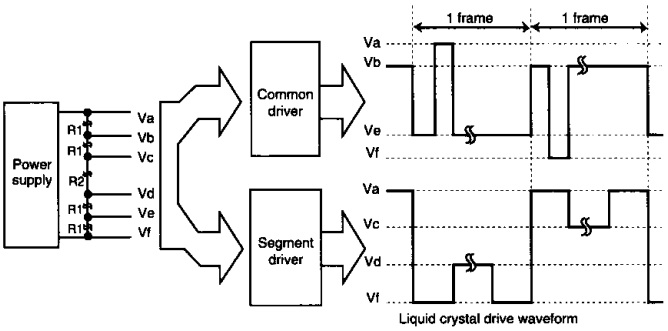


The above figure shows the structure of an LCD. Liquid crystals are placed between two types of glass substrates, one having segment electrodes (SEG1, SEG2, and so on), the other having common electrodes (COM1, COM2, and so on). Each cross point of the segment and common electrodes is a display pixel.

The LCD is driven as follows. The common electrodes are sequentially selected. The display pixels on the selected common electrode are turned on/off according to the select/non-select signals of the corresponding segment electrodes. This is called multiplex drive.

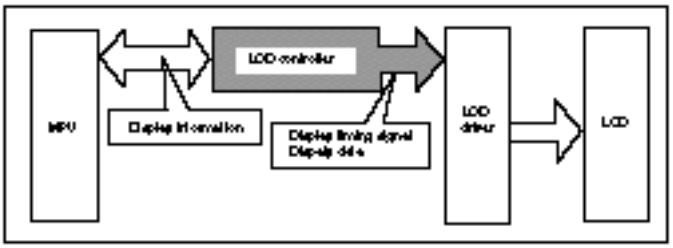


The LCD driver generates liquid crystal drive waveforms according to the display information sent from the MPU, and uses the waveforms to drive the LCD.



The LCD drivers are classified into two types: the common driver and the segment driver. The common driver drives common electrodes and the segment driver drives segment electrodes. As shown in the figure above, these drivers select a proper voltage level sequentially from the six voltage levels (Va to Vf) to generate liquid crystal drive waveforms. The six voltage levels are generated by resistance division.

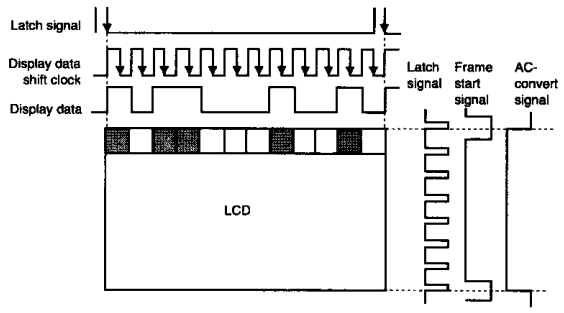
LCD CONTROLLER



The MPU cannot directly interface the LCD driver. So the LCD controller is placed between the MPU and the LCD drivers to handle the interface between them.

The LCD controller receives display information from the MPU, converts it into the display timing signals and display data required for the LCD drivers, and transfers them to the LCD drivers.

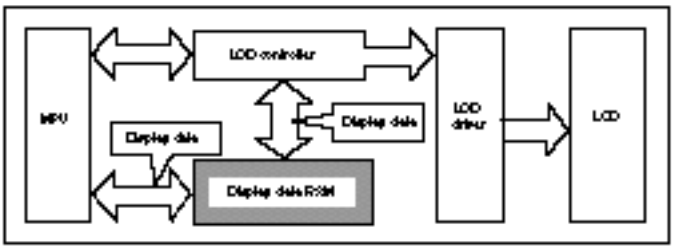
PRINCIPLES OF OPERATION



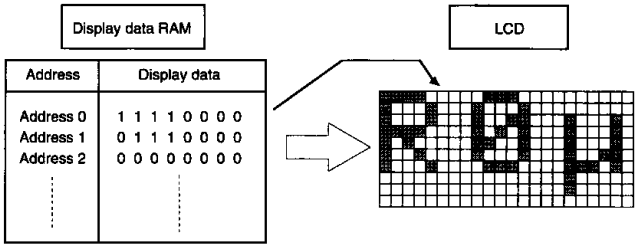
There are four display timing signals: display data shift clock, latch signal, frame start signal, and AC-convert signal.

There are two formats for the display data transfer: serial transfer and parallel transfer. In serial transfer, data is transferred bit by bit as shown in the figure above. In parallel transfer, four or eight bits are transferred at the same time. All **Seiko Instruments** graphic modules use parallel transfer.

DISPLAY DATA RAM

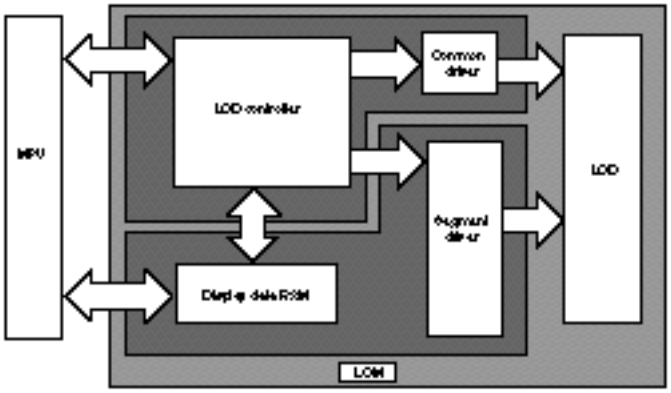


The display data RAM stores the display information sent from the MPU. The LCD controller reads data from the display data RAM, and transfers the data to the LCD drivers. Some LCD controllers let the MPU directly interface the display data RAM as shown by dotted lines in the figure above.



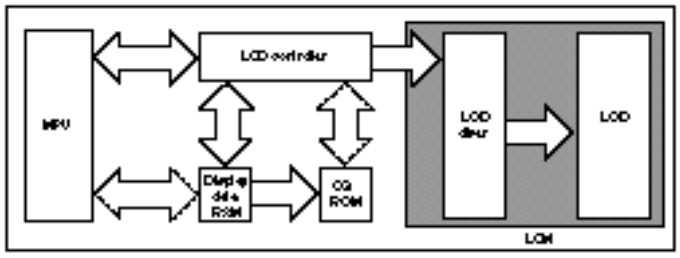
One of the methods to correspond display contents to display data is to assign a display data bit to a display pixel dot. In that case, if the MPU writes and stores data “11110000” at address 0 of the display data RAM, the LCD screen displays a pattern of “■■■■□□□□” according to the 0s and 1s in the data. This correspondence method is called the graphic display mode. The graphic display mode allows any pattern to be displayed, because each display pixel dot can be turned on and off independently.

GRAPHIC LCD MODULE WITH BUILT-IN RAM (G1213, G1216)



Graphic modules with built-in data RAM have two types of ICs: one integrating the controller and common driver, and one integrating the display data RAM and the segment driver. These modules use direct bitmapping; one bit in RAM corresponds to each pixel on the display. They communicate directly to the microprocessor through an 8-bit parallel interface. All the required controller timing functions are built-in to the module. There is no CG ROM, or any way to store information.

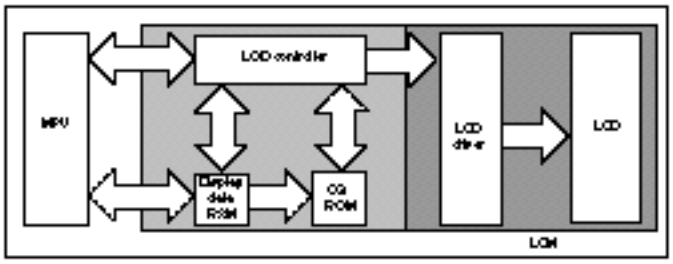
GRAPHIC LCD MODULES WITH EXTERNAL CONTROLLER (G191C, G2436, G321E, G648D, G649D)



Most graphic modules feature the segment and common drivers on the LCD module, and use a 4-bit parallel interface to an external controller. The controller can be an external PC board (such as the LCDC-1330) or the controller IC can be located on the mother board with the microprocessor. In the larger graphic modules, all the board space is taken up with the driver ICs. Also for small graphic modules with high resolution, there may be no room to locate the controller on the module.

PRINCIPLES OF OPERATION

GRAPHIC MODULES WITH BUILT-IN CONTROLLER (G121C, G242C, G321D, G324E)

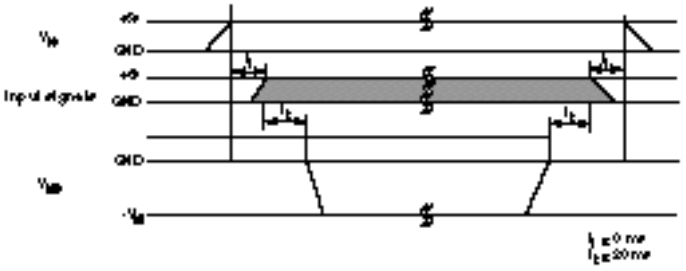


Seiko Instruments offers five graphic modules with the SED1330 controller built-in.* These modules interface directly to the microprocessor with an 8-bit parallel interface. The 1330 was carefully chosen to offer our customers the most advanced features, including overlayed graphics and text, horizontal and vertical scrolling, built-in character generator with external RAM, etc.

* Model G121C features SED1335.

POWER ON / OFF AND SIGNAL INPUT TIMING

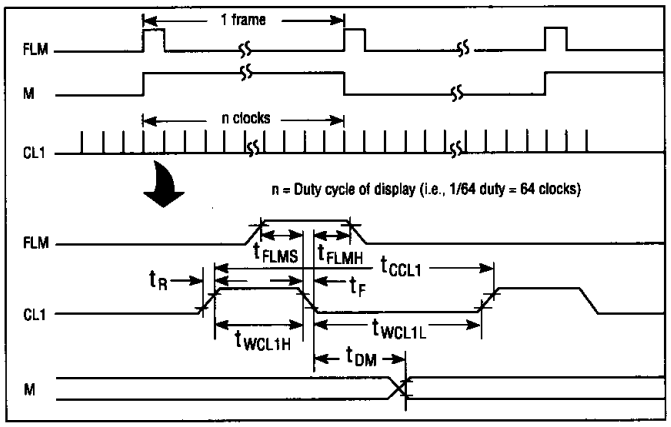
Power ON/OFF and signal input should be performed according to the timing shown below in order not to damage the LCD driving circuit and the LCD panel.



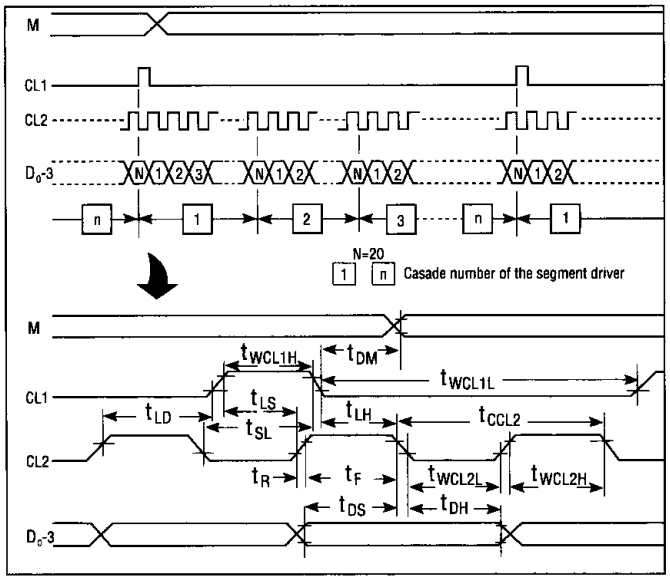
INTERFACE SIGNAL	FUNCTION
A0	Command mode set
CL1	Display data latch signal. Signal is used to latch data in each common line
CL2	Display data shift signal. Clock signal to shift data in 4-bit increments to the display
CS1, CS2	Chip select (read/write enable)
/CS	Chip select
D_0-D_3	Display data signal; D0-D3 for single screen; UD0-UD3 & LD0-LD3 for dual screen display
DB_0-DB_7	Tri-state bidirectional data bus
D/I	Display data/display control data instruction
E	Enable
FLM	Frame start-up signal. Beginning signal that is sent at the start of each screen frame
INHX	Display on/off signal: H=on, L=off
M	Liquid crystal AC signal. This signal provides AC polarity in each display frame to prevent damage to the LCD from DC voltage
/RD	Read
/RES, RST	Reset
RS	Register select signal
R/W	Read/write select signal
SEL1, SEL2	MPU interface configuration; for Intel, SEL 1=0, SEL 2=0; for Motorola, SEL 1=1, SEL 2=0
V_{DD}	Power supply voltage for logic: +5 V
V_{LC}	Power supply for LCD: -5 V to -24 V(see model)
V_0	LCD contrast adjustment voltage
V_{SS}	Ground
/WR	Write

TIMING CHARACTERISTICS

The following timing diagrams apply to all the graphic modules without a built-in controller.



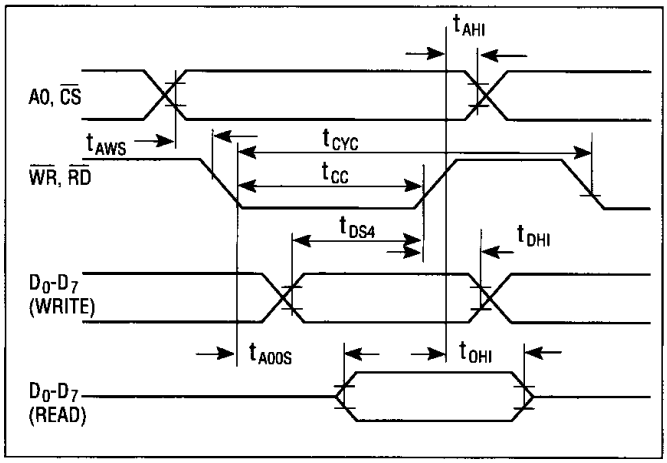
Timing characteristics of signal input into segment driver.



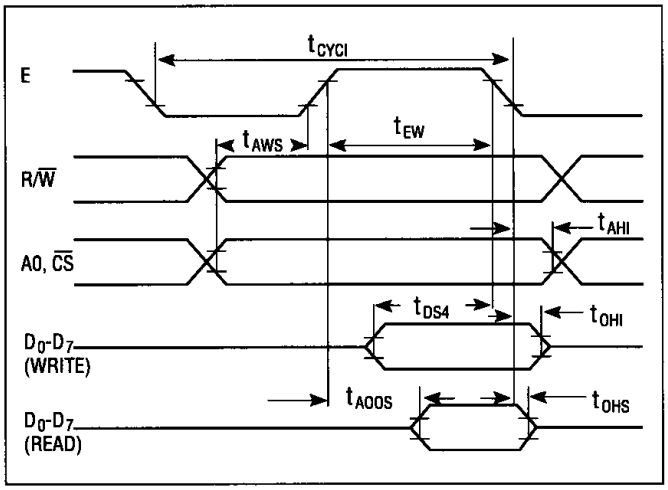
Timing characteristics of signal input into segment driver.

TIMING CHARACTERISTICS TEMP. = 0 - 50°C, V_{DD} = 5.0V ± 5%, V_{SS} = 0V				
Item	**Symbol**	**Min.**	**Max.**	**Unit**
CL1 period	t_{CCL1}	1000		ns
CL1 "H" pulse width	t_{WCL1H}	125		ns
FLM setup time	t_{FLMS}	100		ns
FLM hold time	t_{FLMH}	100		ns
Input signal rise time	t_R		30	ns
Input signal fall time	t_F		30	ns
CL2 period	t_{CCL2}	330		ns
CL2 "H" pulse width	t_{WCL2H}	110		ns
CL2 "L" pulse width	t_{WCL2L}	110		ns
Data setup time	t_{DS}	100		ns
Data hold time	t_{DH}	100		ns
CL2 fall to CL1 fall time	t_{SL}	125		ns
CL1 fall to CL2 fall time	t_{LH}	80		ns

TIMING CHARACTERISTICS FOR MODULES WITH BUILT-IN 1330 CONTROLLER



Intel 80 series timing diagram



Motorola 68 series timing diagram

Signal		Symbol	Item	Min.	Max.	Unit
80 series timing	WR RD	t_{CYC}	System cycle time	1000	-	ns
		t_{CC}	Control pulse width	220	-	ns
68 series timing	A0, CS, R/W,E	t_{CYC}	System cycle time	1000	-	ns
		t_{EW}	Enable pulse width	220	-	ns
80 and 68 series timing	A0, CS	t_{AH}	Address hold time	10	-	ns
		t_{AW}	Address setup time	30	-	ns
	D0-D7	t_{DS}	Data setup time	120	-	ns
		t_{DH}	Data hold time	10	-	ns
		t_{ACC}	RD access time		120	ns
		t_{0H}	Output disable time	10	50	ns

Note: See page 53 for microprocessor chip selection control (SEL).