VLSI Circuits for Wireless Communication

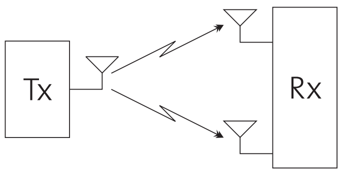
Wireless communication has become one of the fastest growing markets worldwide. The main reasons for this success are global standardization efforts, affordable communication services, and the emergence of low-cost end-user terminals.
The evolution is driven by a continuously growing number of users and new applications which continue to require better quality of service (QoS) and higher data rates.

- Since the spectrum available for wireless communication is limited and unused spectrum is scarce, this **demand can not be met by simply allocating more bandwidth**.
- Therefore next generation wireless communication systems require new algorithms and transmission schemes to satisfy these needs.
- The associated significant increase in signal processing mandates for dedicated hardware solutions. The VLSI design challenge is to provide small and affordable integrated circuits.

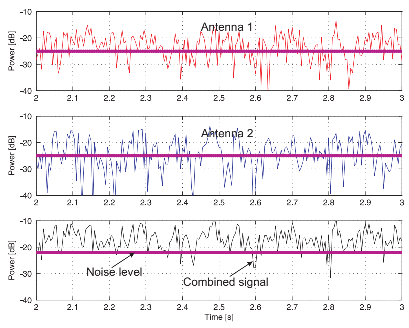
Multiple Antennas Achieve Higher Spectral Efficiency

Using multiple antennas at the receiver

- Stabilizes the link by mitigating the effects of fading through multiple antennas: **diversity gain**
- Improves the received signal-to-noise ratio: **array gain**



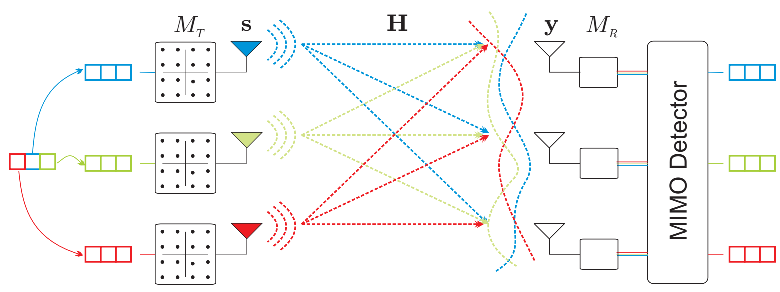
Single-input multiple-output system



Multiple-Input Multiple-Output (MIMO) Systems

Using multiple antennas at the transmitter and the receiver:

- Multiple data streams can be transmitted *concurrently* within the *same frequency band*: **spatial multiplexing**



$$\mathbf{y} = \mathbf{H}\mathbf{s} + \mathbf{n}$$

Benefits of MIMO Communication Systems

- Longer range compared to single-input single-output systems.
- Higher throughput without the need for additional bandwidth.
- Better quality of service (QoS).

VLSI Design Challenges

MIMO technology is a very promising candidate to alleviate performance bottlenecks in wireless communication systems.

- Unfortunately, the tremendous gains associated with MIMO technology come at the expense of a considerable amount of signal processing and hence circuit complexity.
- To enable small and low-cost MIMO communication systems, the **implementation of low-complexity VLSI circuits** is crucial and **poses many research challenges**.

Optimizations to achieve **hardware complexity reductions** can be made on various levels of abstraction: *system level*, *algorithmic level*, *architectural level*, or *circuit level*.

We believe that the **key to the efficient implementation** of MIMO receivers for next generation wireless communication systems is the **joint consideration of algorithmic and VLSI architectural aspects**.

MIMO Research at the Integrated Systems Laboratory

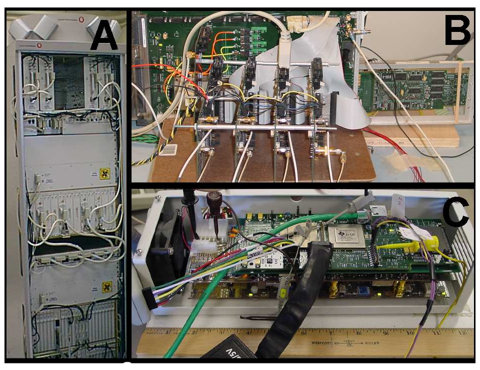
- Personel: 6 PhD students, 1 Postdoc
- Partners: Communication Theory Group (CTG) ETH Zurich
- Past, current and upcoming projects:
  - MIMO-HSDPA testbed (Lucent, ended 2003)
  - **MIMO-WLAN / MIMO-OFDM testbed** (ETHZ)
  - Multi-user MIMO systems (FP6 project MASCOT)
  - Implementation of MIMO algorithms (ETHZ)
  - Reconfigurable architectures for MIMO WLAN (KTI, BridgeCo)

Approach

- Focus on the VLSI integration of digital signal processing blocks.
- Using FPGA prototypes for system development and to **verify algorithm performance under real-world conditions**.
- Developing dedicated ASICs for critical system components.

MIMO-HSDPA Testbed (Lucent/ETHZ-IIS)

In 2000, first proposals have emerged to include MIMO in UMTS and later in HSDPA. In 2002, the first real-time demonstration of MIMO-HSDPA has been developed in collaboration with Bell-Labs/Lucent. The testbed is located at Lucent.

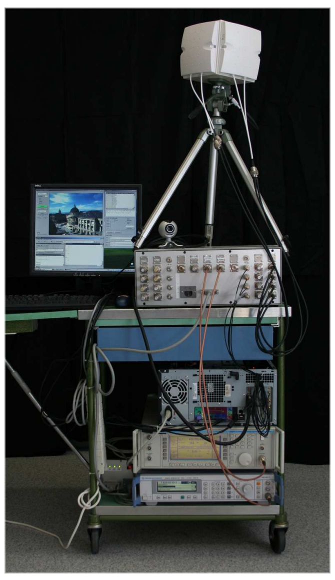


Components developed at ETHZ:

- MIMO-HSDPA baseband processing in FPGAs
- Maximum likelihood MIMO detector
- Equalization algorithms for MIMO-HSDPA

4×4 system achieves 1 Mbps/user for up to 31 users per cell.

Real-Time MIMO-OFDM Testbed (ETHZ-IIS/CTG)



- Research vehicle to develop and test MIMO algorithms:
  - 4×4 MIMO-OFDM system
  - Signal processing on FPGAs
  - 2.4 GHz and 5.2 GHz RF
  - 2 terminals
- **First real-time demonstration of 4-stream MIMO-WLAN**
- System is based on 802.11n

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IIS MIMO