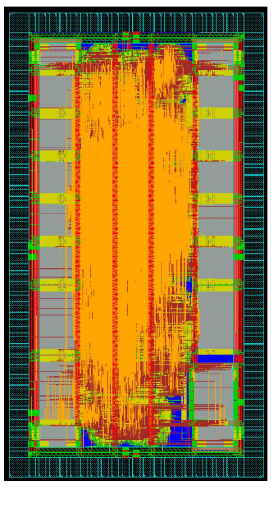
IIS ASICs for Wireless MIMO Communication - Part 2

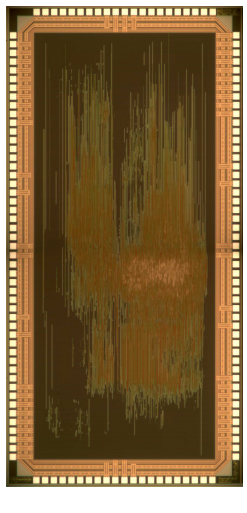
Baseband Processor I for 2×2 MIMO-OFDM



Description
- Baseband processor for 2 × 2 MIMO-OFDM: frame sync and FFT processing

Technical Data
- Process: UMC 0.18 µm 1P/6M CMOS technology
- Clock: 250 MHz
- Area: 3.95 mm^2
- Delivers up to 2 M 64-point FFT/s

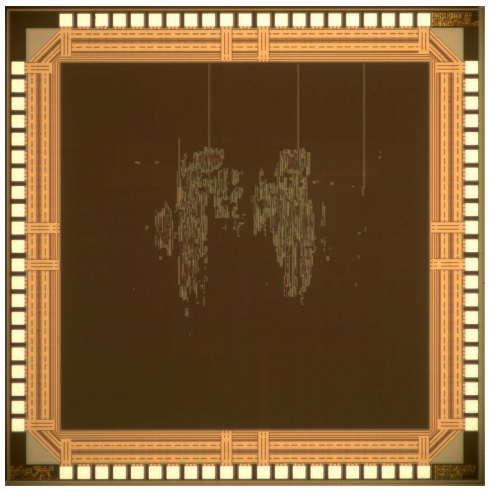
Baseband Processor II for 2×2 MIMO-OFDM



Description
- Computes linear MMSE estimator matrix and performs MIMO detection

Technical Data
- Process: UMC 0.18 µm 1P/6M CMOS technology
- Clock: 185 MHz
- Area: 3.7 mm^2
- Delivers up to 4.2 M MMSE matrices per second

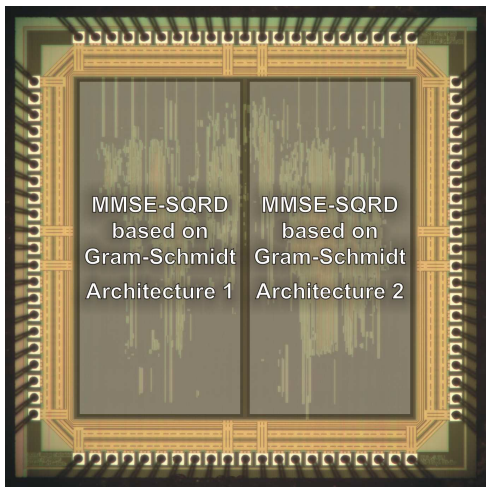
High-Throughput Steering Matrix Computation



Description
- First steering matrix (SM) computation unit for 4×4 MIMO beamforming

Technical Data
- Process: UMC 0.18 µm 1P/6M CMOS technology
- Clock: 149 MHz
- Area: 0.41 mm^2
- Delivers up to 0.3 M SM/s

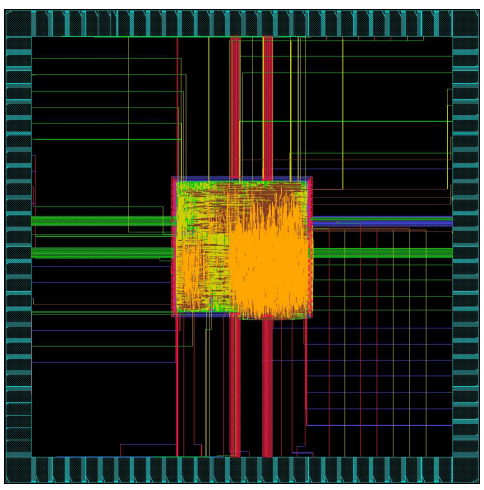
Gram-Schmidt-Based MMSE-SQRD



Description
- Gram-Schmidt-based MMSE sorted QR decomposition

Technical Data
- Process: UMC 0.18 µm 1P/6M CMOS technology
- Clock: 162 MHz
- Area: 0.99 mm^2
- Delivers 1.56 M SQRD/s

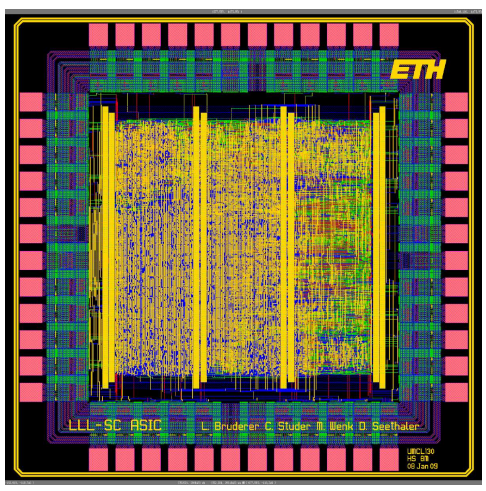
Pipelined Hard-Output Sphere Decoder



Description
- Pipelined sphere decoder with early termination for 4-stream MIMO detection

Technical Data
- Process: UMC 0.13 µm 1P/8M CMOS technology
- Clock: 333 MHz
- Area: 90 k gate equivalents
- Achieves up to 761 Mbit/s

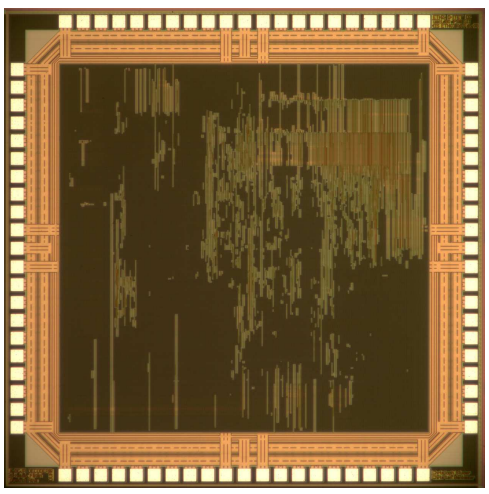
Lattice Reduction ASIC for MIMO Detection



Description
- First ASIC implementation of the LLL algorithm for MIMO detection

Technical Data
- Process: UMC 0.13 µm 1P/8M CMOS technology
- Clock: 303 MHz
- Area: 1.58 mm^2
- Processes up to 5.4 M matrices per second

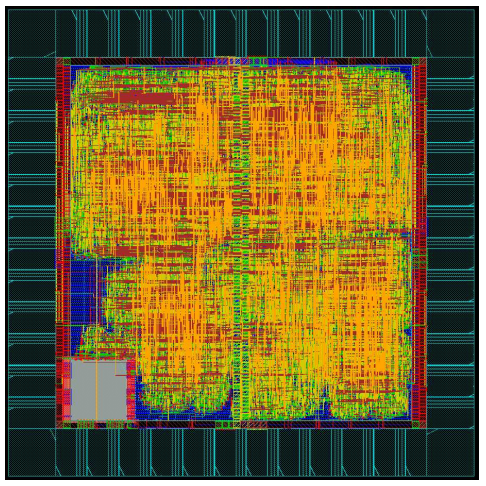
4-, 8-, 16-, and 32-State BCJR Decoder



Description
- 4-, 8-, 16-, and 32-state BCJR decoder for iterative MIMO detection

Technical Data
- Process: UMC 0.18 µm 1P/6M CMOS technology
- Clock: 375 MHz
- Area: 2.90 mm^2
- Throughput: 375 Mbit/s

High-Throughput BCJR Decoder



Description
- 8-state radix-4 BCJR decoder for high-throughput turbo decoding

Technical Data
- Process: UMC 0.18 µm 1P/6M CMOS technology
- Clock: 350 MHz
- Area: 0.76 mm^2
- Throughput: 700 Mbit/s

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