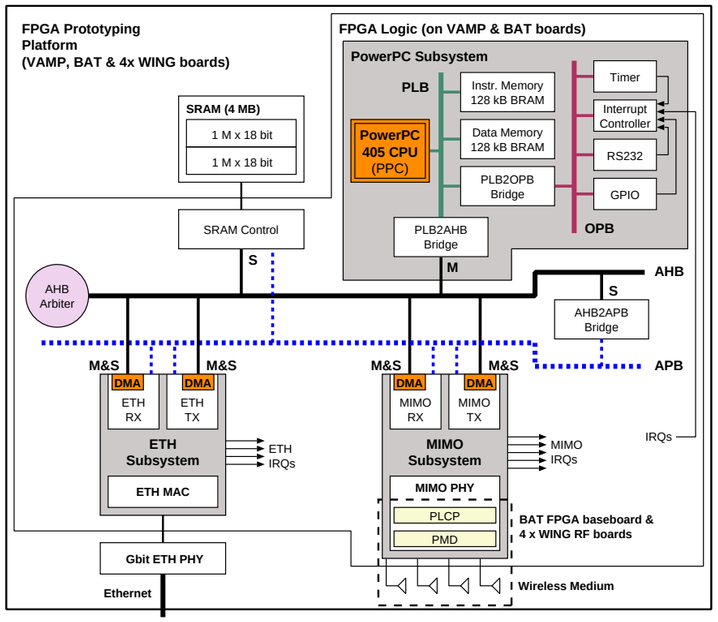
MASCOT Real-Time 4×4 MIMO-OFDM Testbed

FPGA Subsystem



System Outline

- 240 MHz IBM PowerPC 405 (FPGA-internal hard macro)
- MAC-related digital logic on one FPGA
- 4 MB external SRAM

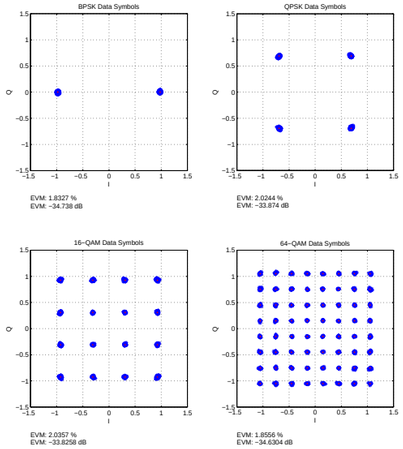
Interconnections

- 80 MHz 64 bit processor local bus (PLB)
- 80 MHz 32 bit system bus (AHB)
- Peripheral bus for configuration (APB)

IBM PowerPC 405 Processor

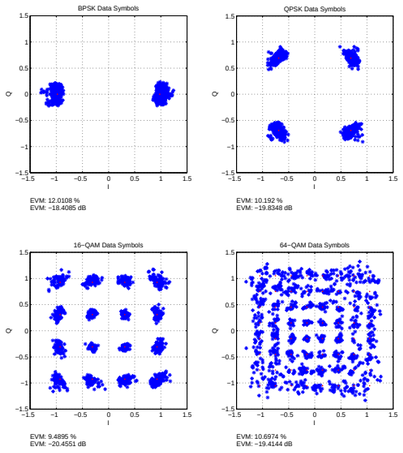
- 32 bit RISC CPU, 32 registers
- 5 stage execution pipeline
- Static branch prediction
- 16 kB 2-way set-associative instruction and data cache
- 2x 128 kB instruction and data memory
- Hardware multiply/divide unit:
  4-cycle integer multiplication
  35-cycle integer division

Constellation Diagrams



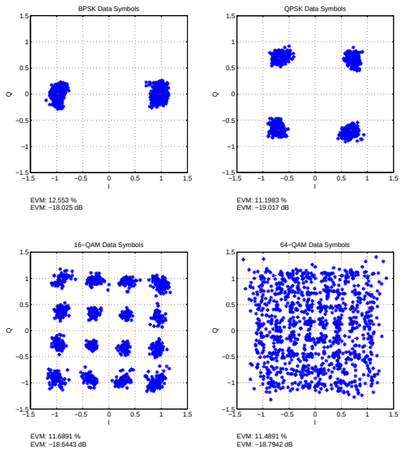
Digital Loopback

Constellation diagrams for different modulation schemes in digital loopback mode (orthogonal channel) – for characterization of the implementation loss in the digital domain.



Coaxial Cable

Constellation diagrams for different modulation schemes across a coaxial cable (orthogonal channel) – for characterization of impairments caused by RF imperfections, e.g., frequency offset or phase noise.



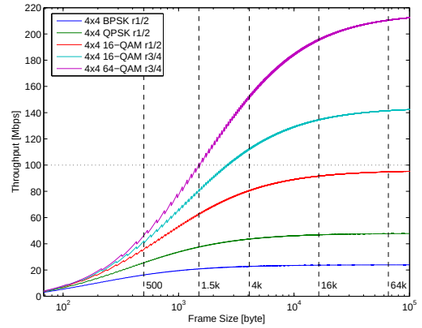
Real-World

Constellation diagrams for different modulation schemes across a real-world wireless MIMO channel – revealing real-world propagation effects such as fading or interference.

Raw MAC-Layer Throughput

Assumptions: entire MAC protocol overhead, perfect channel state information, no interference, no outage, no errors, no retransmissions

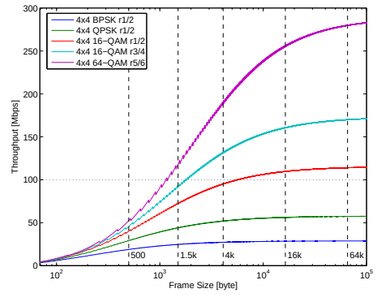
MASCOT Testbed



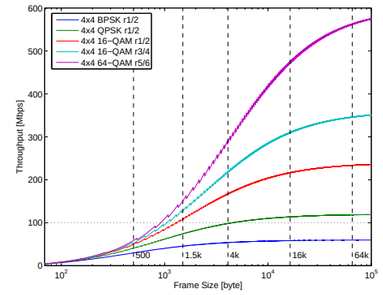
Constraints

- 48 data subcarriers
- 0.8 µs guard interval
- 16 µs interframe space
- 44 µs PHY header
- 32 byte MAC header, 4 byte FCS

IEEE 802.11n, 20 MHz, 52 sc.

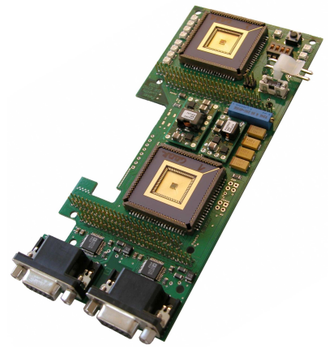


IEEE 802.11n, 40 MHz, 108 sc.



Constraints: 0.4 µs guard interval, 16 µs interframe space, 40 µs PHY header (HT-GF), 3 byte service, tail, and padding, 30 byte MAC header, 4 byte FCS

Future Work



- Testbed integration of MMSE sorted QR decomposition (SQRD) ASIC for MIMO preprocessing.
- FPGA implementation of advanced MIMO detection algorithms, i.e., near-ML or ML performance-achieving detection schemes.
- Implementation of simultaneous collision-based multi-user MIMO transmission schemes.

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IIS MIMO